PTO-1449 REPRODUCED	ATTORNEY DOCKET NO.	APPLICATION NO.
SUPPLEMENTAL INFORMATION DISCLOSURE CITATION IN AN APPLICATION	2037.1004-007	10/645,330
	FIRST NAMED INVENTOR: Richard C. Foss	FILING DATE: August 21, 2003
August 18, 2004	EXAMINER: Michael T. Tran	CONFIRMATION NO.: 7565 / GROUP: 2818
(Use several sheets if necessary)		

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	REF. NO.	DOCUMENT NUMBER Number-Kind Code (if known)	ISSUE DATE / PUBLICATION DATE MM-DD-YYYY	CLS	SUB	NAME OF PATENTEE OR APPLICANT OF CITED DOCUMENT
MT	AC2	4,623,805	11-18-1986	327	152	Flora et al.
	AD2	4,755,704	07-05-1988	327	152	Flora et al.
	AE2	4,338,569	07-06-1982	327	158	Petrich
	AF2	4,604,582	08-05-1986	327	147	Strenkowski et al.
	AG2	4,637,018	01-13-1987	714	700	Flora et al.
	AH2	5,272,729	12-21-1993	375	371	Bechade et al.
MT	AI2	4,330,852	05-18-1982	365	221	Redwine et al.

EXAMINER	DATE CONSIDERED
M. TRAN	10/16/04

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OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent Pages, Etc.)*		
MT	AV	Hatakeyama, Atsushi, et al., "A 256Mb SDRAM Using a Register-Controlled Digital DLL," Fujitsu Limited, Kawasaki, Japan.
MT	AW	Hatakeyama, Atsushi, et al., "A 256-Mb SDRAM Using a Register-Controlled Digital DLL," *IEEE Journal of Solid-State Circuits,* Vol. 32, No. 11, pp. 1728-1734 (November 1997).
	AX	Efendovich, Avner, et al., "Multifrequency Zero-Jitter Delay-Locked Loop," *IEEE Journal of Solid-State Circuits,* Vol. 29, No. 1, pp. 67-70 (January 1994).
	AY	Choi, Yunho, et al., "16Mbit Synchronous DRAM with 125Mbyte/sec Data Rate," 1993 Symposium on VLSI Circuits Digest of Technical Papers, pp. 65-66, (1993).
MT	AZ	Lee, Thomas H., et al., "A 2.5V Delay-Locked Loop for an 18Mb 500MB/s DRAM," IEEE International Solid-State Circuits Conference, Session 18, pp. 300-301 (February 18, 1994).
	AR2	Takai, Yasuhiro, et al., "250 Mbyte/s Synchronous DRAM Using a 3-Stage-Pipelined Architecture," *IEEE Journal of Solid-State Circuits,* Vol. 29, No. 4, pp. 426-431 (April 1994).
	AS2	Choi, Yunho, et al., "16-Mb Synchronous DRAM with 125-Mbyte/s Data Rate," *IEEE Journal of Solid-State Circuits,* Vol. 29, No. 4, pp. 529-533 (April 1994).
MT	AT2	Takai, Y., et al., "250 Mbyte/sec Synchronous DRAM Using a 3-Stage-Pipelined Architecture,"1993 Symposium on VLSI Circuits Digest of Technical Papers, pp. 59-60, (1993).

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